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(54) Improvements in or relating to semiconductor devices

(57) An isotropic or partially isotropic etch shrinks lithographically patterned photoresist (211, 212) to yield reduced linewidth patterned photoresist (213, 214) with a buried antireflective coating also acting as an etchstop or a sacrificial layer. The reduced linewidth pattern (213,

214) provide an etch mask for subsequent anisotropic etching of underlying material such as polysilicon (206) or metal or insulator or ferroelectric.

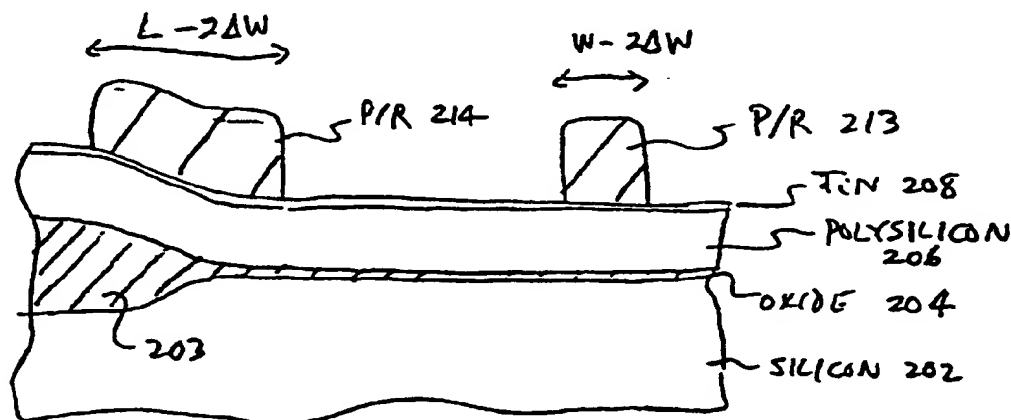


Fig. 2e

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Descripti n

BACKGROUND OF THE INVENTION

The invention relates to semiconductor devices, and, more particularly, to fabrication methods for such devices.

Semiconductor integrated circuits with high device density require minimum size structures such as short gates for field effect transistors (FETs), small area emitters for bipolar transistors, and narrow interconnection lines between devices. The formation of such polysilicon or metal structures typically involves definition of the locations of such structures in a layer of photoresist on a layer of polysilicon or metal by exposure of the photoresist with light passing through a reticle containing the desired structure pattern. After exposure and development of the photoresist, the underlying layer of polysilicon or metal is anisotropically etched using the patterned photoresist as the etch mask. Thus the minimum polysilicon or metal linewidth equals the minimum linewidth that can be developed in the photoresist. Current optical steppers expose the photoresist using light of wavelength 365 nm (called I-line after the corresponding emission line in a high-pressure mercury arc lamp used to generate the light), and pattern linewidths in photoresist of less than about 0.30 μm with a standard deviation of less than about 0.01 μm cannot be satisfactorily generated with I-line lithography.

Figures 1a-c illustrate a known method to create sublithographic polysilicon gate structures and includes minimal geometry patterning photoresist on a polysilicon layer (Figure 1a), isotropically etching the photoresist to reduce linewidth (Figure 1b), and anisotropically etching the polysilicon with the reduced linewidth photoresist as etch mask (Figure 1c). This approach has problems including contamination of the polysilicon.

The use of a photoresist mask for anisotropic etching polysilicon gates can leave residual ridges of hardened photoresist on the edges of the polysilicon gates after the etch. Plasma etch species harden the photoresist sidewalls during the polysilicon etch, and the subsequent oxygen plasma photoresist strip may not fully remove the ridges; Figure 1d. Also, separate wet etches to strip the ridges may be used but lack robustness with respect to modifications. Any ridge residue will carbonize during later heat treatments and impede formation of titanium disilicide (TiSi_2) in a self-aligned gate silicication process. Thus simple and complete removal of photoresist residue is a problem.

SUMMARY OF THE INVENTION

The present invention provides sublithographic patterns by use of an intermediate layer between photoresist and material to be etched together with lateral etching of either a lithographically defined photoresist pattern or the intermediate layer to shrink the linewidth. The intermediate layer acts as (1) an antireflective layer

for photoresist exposure, (2) as an etchstop or as a sacrificial layer for the subsequent lateral etch, and/or (3) a liftoff layer for removal of hardened photoresist residue.

Accordingly, the present invention provides a method of lithography comprising, providing a first layer to be patterned, forming an intermediate layer over said first layer, forming a radiation sensitive layer overlying said intermediate layer, patterning said radiation sensitive layer with radiation, removing portions of said intermediate layer to form a first patterned region substantially underlying said radiation sensitive layer, removing portions of said first patterned region to form a second patterned region, and removing portions of said first layer using said second patterned region as at least a portion of a mask.

Advantages of the invention include a simple method for sublithographic patterns and robust photoresist removal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described by way of example, with references to the accompanying drawings in which;

Figures 1a-d show a known sublithographic pattern method;

Figures 2a-h illustrate a first preferred embodiment of the method of the present invention for photoresist patterning in cross sectional elevation and plan views;

Figure 3 is a cross sectional elevation view after an anisotropic etch using the method illustrated in Figures 2a-h;

Figures 4a-d illustrate a second preferred embodiment method of the present invention for photoresist patterning;

Figure 5 illustrates etch selectivity;

Figure 6 illustrates a polysilicon etch;

Figures 7a-b show a cross sectional elevation view of a third preferred embodiment method of the present invention;

Figures 8a-e are cross sections of a fourth preferred embodiment method of the present invention, and

Figure 9a-d illustrate in cross sectional elevation views of a fifth preferred embodiment method of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Overview

The preferred embodiment methods of sublithographic pattern creation insert an intermediate layer between photoresist and the material to be patterned and use the following steps: first expose and develop a pattern in the photoresist with a minimal linewidth and then laterally (e.g., isotropically) remove photoresist or intermediate layer or both to uniformly shrink the intermediate layer to a subminimal linewidth which then provides the etch mask for the material to be patterned. The intermediate layer may provide (1) an anti-reflection function during photoresist exposure, (2) an etchstop or a sacrificial layer to protect the underlying material layer during the subsequent lateral removal, and/or (3) an etch residue liftoff layer after the material has been patterned.

The sublithographic patterning and residue liftoff can be created over materials such as polysilicon, metal, insulator, ferroelectric, and so forth. The sublithographic pattern may define minimal sized items such as gate length and interconnection linewidth for integrated circuits.

FIRST PREFERRED EMBODIMENT

Figures 2a-h illustrate the first preferred embodiment photoresist patterning method as could be used to form a mask for gate level polysilicon etching. In particular, begin with monocrystalline silicon substrate 202 having (100) orientation and typically with both p and n type doped well regions for fabrication of devices plus also isolation oxides 203, gate oxide 204 with thickness typically 6-10 nm plus gate level polysilicon layer 206 with thickness typically 300-500 nm and either doped or undoped or doped only in certain portions. Then proceed with the following steps:

(1) Sputter deposit a 55 nm thick layer 208 of titanium nitride (TiN) onto polysilicon 206. TiN layer 208 acts as a buried anti-reflective coating ("BARC") for I-line lithography; that is, TiN strongly absorbs 365 nm wavelength light. Without TiN or some other BARC, the underlying polysilicon 206 would reflect exposure light penetrating overlying photoresist and cause interference which makes the photoresist's degree of exposure depend upon location because the photoresist thickness varies over protuberances such as isolation oxide 203.

(2) Spin on roughly 1 μm thick I-line photoresist layer 210 onto TiN BARC 208; the thickness of layer 210 depends on the underlying topography. I-line photoresist may be made of cyclized polyisoprene polymers with azide sensitizers. Softbake photoresist 210 if desired. See Figure 2a-b for cross sec-

tional elevation and plan views.

(3) Expose photoresist 210 with an I-line lithography system to define a pattern with minimum linewidth of 0.33 μm . Then develop exposed photoresist 210 and bake to yield patterned photoresist portions 211 and 212 as illustrated in Figure 2c-d in cross sectional elevation and plan views. The width denoted "W" may be a minimum line width such as 0.33 μm . See Figures 2c-d with Figure 2c being the section along line C-C in plan view Figure 2d.

(4) Apply an isotropic etch to remove ΔW of photoresist patterns 211-212 to yield photoresist patterns 213-214, but the etch only removes a negligible amount of TiN 208. This isotropic etch may be a plasma etch with 80% helium and 20% oxygen at a pressure of 1.5 mTorr which removes photoresist at a rate of 160 nm/min. Thus a 15 second etch would remove 0.04 μm of photoresist and reduce a 0.33 μm linewidth down to a 0.25 μm linewidth. See Figures 2e-f which show the etched photoresist patterns 213-214 defining a linewidth of $W-2\Delta W$ with solid lines together with the original photoresist patterns 211-212 defining a linewidth of W with broken lines.

(5) Apply an anisotropic etch to remove the exposed portions of TiN layer 208 and complete the etch mask for etching polysilicon 206. A helicon plasma etcher with chlorine at a pressure of 6 mTorr will etch TiN at about 200 nm/min, so an etch of roughly 15 seconds will remove exposed TiN to leave TiN portions 217-218. This etch will also etch polysilicon at roughly the same rate, but stopping in polysilicon 206 is not critical because polysilicon 206 will be anisotropically etched next anyway. Figures 2g-h illustrate the final photoresist patterns 213-214 on underlying TiN portions 217-218 which form the mask with $W-2\Delta W$ minimum linewidth to be used for anisotropic etching of polysilicon 206.

The anisotropic etching of polysilicon 206 then proceeds with a helicon excited plasma from a gas mixture of Cl_2 , HBr, and He/O_2 (80%/20%) at a pressure of about 6 mTorr and using the photoresist patterns 213-214 as etch mask. The Br provides sidewall passivation to insure anisotropy. $\text{Cl}_2/\text{HBr}/\text{He-O}_2$ plasma may etch polysilicon about 300 times faster than oxide, and an overetch on oxide 204 will only remove a minimal amount of oxide; see Figure 3. A final oxygen plasma strips the photoresist plus a chlorine plasma or an SC1 rinse ($\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ solution) strips the TiN from the etched polysilicon without affecting either the polysilicon or the exposed gate oxide.

SECOND PREFERRED EMBODIMENT

Figures 4a-d illustrate the second preferred embod-

iment 7 resist patterning method as could also be used to a mask for gate level polysilicon etching. In particular, again begin with monocrystalline silicon substrate 400 having (100) orientation with isolation oxides 403, gate oxide 404 with thickness 6 nm plus gate level polysilicon layer 406 with thickness 400 nm. Then proceed with the following steps:

(1) Spin on a 200 nm thick layer 408 of organic BARC onto polysilicon 406. That is, organic BARC layer 408 strongly absorbs 365 nm wavelength light. Organic BARC 408 may be a polymer with attached dye groups which provide the absorption but without change in polymer bonds; for example, polyamic acid polymers and copolymers. As previously noted, without some sort of BARC, the underlying polysilicon 406 would reflect exposure light penetrating overlying photoresist 410 and cause interference which would make the photoresist's degree of exposure depend upon location because the photoresist thickness varies.

(2) Spin roughly 1 μm thick photoresist layer 410 onto BARC layer 408; the thickness of layer 410 depends on the underlying topography. See Figure 4a for a cross sectional elevation view.

(3) Expose photoresist 410 with an I-line lithography system to define a pattern with minimum linewidth of 0.30 μm . Then develop the photoresist and bake to yield patterned photoresist portions 411 and 412 as illustrated in Figure 4b. The width denoted "W" may be a minimum linewidth such as 0.30 μm .

(4) Etch using a mixture of $\text{CHF}_3/\text{CF}_4/\text{O}_2$ or CHF_3/O_2 at a pressure of 25-75 mTorr in a parallel plate plasma etcher to anisotropically remove the exposed portion of BARC layer 408. This etch also removes photoresist isotropically with a rate dependent upon the CHF_3 to CF_4 ratio: a mixture of CHF_3 and O_2 removes photoresist (which may be based on a polymer of isoprene) at roughly the same rate as it removes BARC, whereas CF_4 and O_2 does not rapidly remove photoresist. Figure 5 suggests the photoresist-to-BARC etch ratio as a function of gas mixture. Thus by selecting the gas mixture, ΔW of photoresist patterns 411-412 can be removed during the BARC etch for any desired ΔW from 0 up to 200 nm to yield photoresist patterns 413-414 with linewidth $W-2\Delta W$. For example, the lithographically defined linewidth of 0.30 μm can be reduced down to a 0.25 μm linewidth during the BARC removal with overetch if the lateral etch rate of photoresist is about 1/10 the vertical etch rate of BARC. See Figures 4c-d which show the lateral and vertical etches and the etched photoresist patterns 413-414 defining a mask with linewidth of $W-2\Delta W$ for etching polysilicon 406.

The etching of polysilicon 406 then proceeds with a plasma from a gas mixture of SF_6 plus HBr using the photoresist patterns 413-414 as etch mask. The Br provides sidewall passivation for anisotropy. Further, the BARC etch of step (4) deposits material 450 on the BARC sidewall as illustrated in Figure 4d; and during the polysilicon etch this sidewall material migrates down the forming polysilicon sidewall as illustrated in Figure 6 and limits microtrenching at the sidewall base. Use a $\text{Cl}_2/\text{HBr}/\text{He}-\text{O}_2$ plasma etch to finish and overetch because this mixture etches polysilicon about 300 times faster than oxide, and an overetch on oxide 404 will only remove a minimal amount of oxide. A final oxygen plasma strips the patterned photoresist plus BARC.

Various anisotropic polysilicon etches have differing amounts of intrinsic linewidth reduction. Consequently, use of the second preferred embodiment allows compensation for the polysilicon etch by adjusting the BARC etch gas mixture so that the total linewidth reduction (photoresist linewidth reduction by BARC etch plus linewidth reduction by polysilicon etch) remains constant.

THIRD PREFERRED EMBODIMENT

The third preferred embodiment again uses an isotropic etch to reduce the minimum linewidth of a photoresist mask with TiN antireflective coating in the case of a metal etch. In particular, aluminum interconnections often have TiN cladding to act as diffusion barriers and electromigration suppressors. Thus Figure 7a shows silicon substrate 702 with insulated gate 704 and planarized oxide insulation 706 having a tungsten filled via 708 connecting down to the source/drain of the FET with gate 704 plus layer 712 of aluminum clad by layers 710 and 714 of TiN.

Next, spin on photoresist 720 and expose with masked I-line light for a pattern with linewidth W; top TiN cladding 714 acts as the anti-reflective coating. Develop photoresist 720 and then apply an oxygen plasma etch to shrink patterned photoresist 720 linewidth to $W-2\Delta W$ using the top TiN cladding 714 as an etchstop; see Figure 7b showing the patterned photoresist shrinkage.

Then apply a chlorine based anisotropic etch to remove TiN 714, Al 712, and TiN 710 not masked by patterned photoresist 720. Strip the patterned photoresist 720 with an oxygen plasma. In this case the structural layer of TiN 714 also acted as the buried anti-reflective coating and the photoresist linewidth shrink etchstop.

FOURTH PREFERRED EMBODIMENT

Figures 8a-d illustrate the fourth preferred embodiment method as could also be used to form a mask for gate level polysilicon etching. In particular, again begin with monocrystalline silicon substrate 802 having (100) orientation with isolation oxides 803, gate oxide 804 with thickness 6 nm plus gate level polysilicon layer 806

with thickness 400 nm. Then proceed with the following steps:

(1) Deposit a 200 nm thick TiN layer 808, which acts as I-line BARC, onto polysilicon 806. TiN deposition may be by sputtering Ti in a N₂ plasma or sputtering TiN. As previously described, BARC 808 limits reflective interference in an overlying photoresist layer which would otherwise make the photoresist's degree of exposure depend upon location because the photoresist thickness varies.

(2) Spin roughly 1 μm thick photoresist layer 810 onto BARC layer 808; the thickness of layer 810 depends on the underlying topography. See Figure 8a for a cross sectional elevation view.

(3) Expose photoresist 810 with an I-line lithography system to define a pattern with minimum linewidth of 0.30 μm. Then develop the photoresist and bake to yield patterned photoresist portions 811 and 812 as illustrated in Figure 8b. The width denoted "W" may be a minimum linewidth such as 0.30 μm.

(4) Apply an anisotropic etch to remove the exposed portions of BARC layer 808; see Figure 8c. For TiN BARC a helicon plasma etcher with chlorine at a pressure of 6 mTorr will etch TiN at about 200 nm/min, so an etch of roughly 60 seconds will remove exposed TiN to leave BARC portions 821-822. This etch will also etch polysilicon at roughly the same rate, but stopping at polysilicon 806 is not critical because polysilicon 806 will be anisotropically etched in step (6).

(5) Apply a timed isotropic etch to laterally remove about 0.025 μm of BARC 821-822 to form narrowed BARC portions 823-824 of minimal width 0.25 μm; see Figure 8d showing the minimal linewidth of W-2ΔW. The isotropic etch for TiN BARC may be a wet etch of dilute H₂O₂ which etches TiN at about 5 nm/min, so this would be a 5 minute etch. Note that overlying photoresist 811-812 limits the amount of BARC exposed to any etchant and thereby greatly diminishes proximity effects to insure a uniform removal of the lateral 0.025 μm of BARC over an entire wafer. Similarly, an isotropic plasma etch could be used. The narrowed BARC 823-824 forms the final etch mask with W-2ΔW minimum linewidth to be used for anisotropic etching of polysilicon 806.

(6) First strip overlying photoresist 811-812 with an oxygen plasma, and then anisotropically etch polysilicon 806 with the BARC 823-824 as etch mask. Note that the thickness of BARC 823-824 permits use of a somewhat nonselective anisotropic polysilicon etch; that is, a plasma etch may also remove the BARC provided that it removes the polysilicon

at least twice as rapidly. See Figure 8e. Lastly, strip the BARC to leave the sublithographically patterned polysilicon.

Note that use of an organic BARC would also be possible provided that the photoresist could be removed without also removing the BARC.

FIFTH PREFERRED EMBODIMENT

Figures 9a-d illustrate the fifth preferred embodiment method as could also be used with any of the foregoing preferred embodiment linewidth reduction methods or could be used without them. The fifth preferred embodiment uses the intermediate layer (possibly BARC) as a liftoff to remove the overlying photoresist or photoresist residue according to the following steps.

(1) Begin with patterned photoresist 911-912 on 50 nm thick TiN intermediate layer portions 917-918 which, in turn, lie on 300 nm thick polysilicon 906. The TiN acted as the BARC for the patterning of the photoresist and, optionally, photoresist 911-912 may have been isotropically etched to shrink linewidth analogous to the structure of Figure 2g. See Figure 9a.

(2) Anisotropically etch polysilicon 906 with a Cl and Br based plasma with photoresist 911-912 plus TiN 917-918 as the etch mask. The etch plasma also forms hardened photoresist portions 913-914 from the sidewalls of photoresist 911-912. See Figure 9b.

(3) Dissolve TiN 917-918 in a solution such as SC1 (1 part 29% NH₄OH, 1 part 30% H₂O₂, and 6 parts H₂O); this also lifts off photoresist 911-912 along with hardened sidewall portions 913-914. See Figure 9c. Optionally, prior to dissolution of TiN 917-918, ash photoresist 911-912 with an oxygen plasma and then dissolve TiN 917-918. This prior ashing exposes another surface of TiN 917-918 for quicker dissolution and still permits liftoff of the hardened sidewall portions 913-914 which the oxygen plasma fails to remove. See Figure 9d which shows the structure after photoresist ashing but prior to the TiN dissolution.

Intermediate layer 917-918 may have been an organic BARC layer, and the method would follow the same steps with BARC dissolution by organic solvent providing the liftoff of the hardened sidewall portions 913-914. However, organic BARC sidewalls would likely also become hardened, so dissolution may require a particular solvent adapted to the type of BARC used. And using an intermediate layer under photoresist for liftoff of hardened sidewalls also applies to etching metal levels, analogous to the third preferred embodi-

ment, and to etching vias through insulators.

MODIFICATIONS AND VARIATIONS

The preferred embodiments may be varied in many ways while retaining one or more of the features of use of an intermediate layer which may act as a buried anti-reflective coating, as an etchstop or sacrificial layer for linewidth reduction, and as a liftoff for overlying photoresist or residue or other material.

For example, the photoresist of the first, second, and third preferred embodiments could be stripped and the patterned BARC alone used as the etch mask provided the etch is selective enough with respect to the BARC. The isotropic etch to reduce photoresist linewidth could be somewhat anisotropic provided sufficient photoresist remains. The layer thicknesses and linewidths and etch chemistries and conditions could all be varied. Further, the preferred embodiment descriptions all used I-line lithography, whereas with other exposure wavelengths using the same or different photoresist and anti-reflective coatings the same approach works. Further, variations could use a single wafer helicon plasma etcher or other types of plasma etchers including batch RIE, ECR RIE, and inductively coupled plasmas.

Claims

1. A method of lithography comprising;
 - providing a first layer to be patterned;
 - forming an intermediate layer over said first layer;
 - forming a radiation sensitive layer overlying said intermediate layer;
 - patterning said radiation sensitive layer with radiation;
 - removing portions of said intermediate layer to form a first patterned region substantially underlying said radiation sensitive layer;
 - removing portions of said first patterned region to form a second patterned region; and
 - removing portions of said first layer using said second patterned region as at least a portion of a mask.
2. The method of claim 1, wherein said step of removing portions of said intermediate layer comprises removing exposed portions of said intermediate layer.
3. The method of Claim 1 or Claim 2 further comprising the steps of; forming said intermediate layer from TiN; and forming said radiation sensitive layer from photoresist.
4. The method of any of Claims 1 to 3, wherein said step of removing portions of said first patterned region is performed by plasma etching.
5. The method of any preceding claim further comprising the steps of;
 - forming said first layer from polysilicon; and
 - removing portions of said first layer by anisotropic plasma etching.
6. The method of any preceding claim, wherein said step of forming said intermediate layer comprises the step of; forming a buried anti-reflective coating (BARC) layer on said first layer, said buried anti-reflective coating layer being absorptive of radiation of a first wavelength.
7. The method of Claim 6, wherein said step of forming a radiation sensitive layer comprises; forming a photoresist layer on said buried anti-reflective coating layer, said photoresist layer being exposed by radiation of the said first wavelength.
8. The method of Claim 7, wherein said step of patterning said radiation sensitive layer comprises;
 - patterning said photoresist layer using radiation inclusive of said first wavelength to form said patterned region in said photoresist layer.
9. The method of Claim 8, wherein the step of patterning said photoresist layer comprises patterning said photoresist layer such that said first patterned region is formed in said photoresist layer having a minimum linewidth W.
10. The method of Claim 8 or Claim 9, wherein said step of removing portions of said intermediate layer comprises; etching said buried anti-reflective coating layer using said patterned photoresist layer to form a first patterned buried anti-reflective coating region.
11. The method of Claim 10, wherein said step of etching said buried anti-reflective coating layer comprises using an anisotropic etching technique.
12. The method of any of Claims 8 to 11, wherein said step of removing portions of said first patterned region comprises; etching said first patterned buried anti-reflective coating layer to remove at least a portion of a surface of said first patterned buried anti-reflective coating layer.
13. The method of Claim 12, wherein said etching step comprises etching said first patterned anti-reflective coating layer using isotropic etching technique.
14. The method of Claim 12, wherein said etching step comprises etching said first patterned anti-reflective coating layer using an anisotropic etching technique.

15. The method of Claim 13 or Claim 14 wherein said etching step comprises etching said first patterned buried anti-reflective coating layer to remove an amount ΔW from a surface of said first patterned buried anti-reflective coating layer to form a second buried anti-reflective coating layer. 5
16. The method of Claim 15, wherein said etching step comprises etching said first patterned buried anti-reflective coating layer to form a second patterned anti-reflective coating layer having a minimum linewidth $W-2\Delta W$ on said first layer. 10
17. The method of Claim 15 or Claim 16 wherein said step of removing portions of said first layer comprises; etching said first layer using said second patterned anti-reflective coating layer as the mask. 15
18. The method of Claim 11 or Claim 12; wherein said step of etching said buried anti-reflective coating layer comprises etching said buried anti-reflective coating layer to form a first patterned buried anti-reflective coating layer having a minimum linewidth W in a region substantially underlying said patterned photoresist layer. 20 25
19. The method of Claim 12 or Claim 13; wherein said step of etching said first layer comprises etching said first layer using said patterned buried anti-reflective coating layer and patterned layer of photoresist as an etch mask. 30
20. The method any of Claims 8 to 19 comprising the step of; stripping said patterned layer of photoresist. 35
21. The method of Claim 20 further comprising the step of; removing said patterned buried anti-reflective coating layer such that substantially all residue from said stripping step is lifted off with removal of said patterned anti-reflective coating layer. 40

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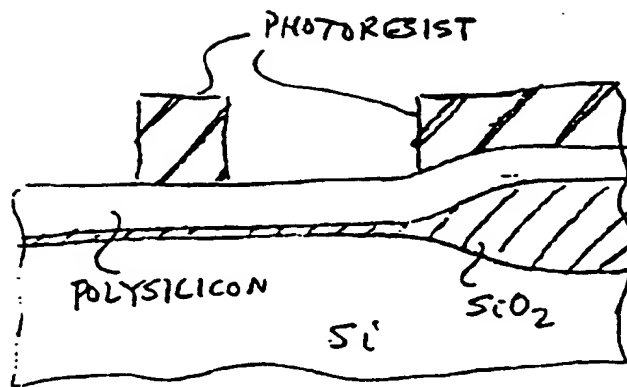


Fig. 1a

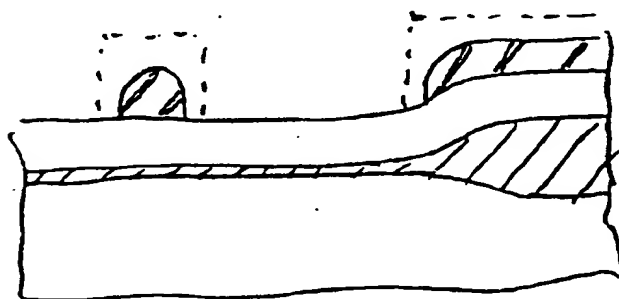


Fig. 1b

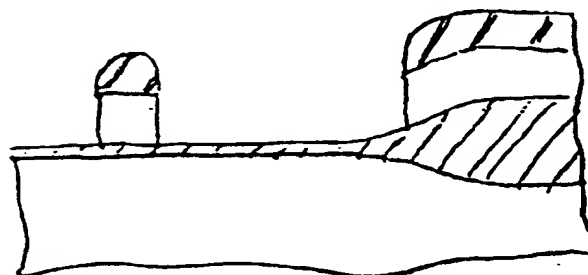


Fig. 1c

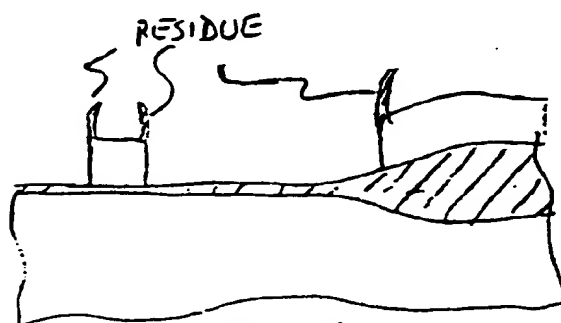


Fig. 1d

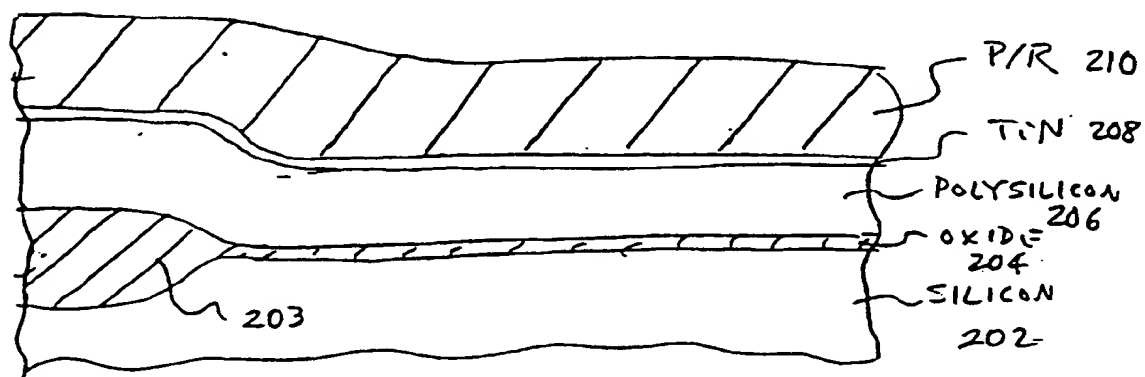


Fig. 2a

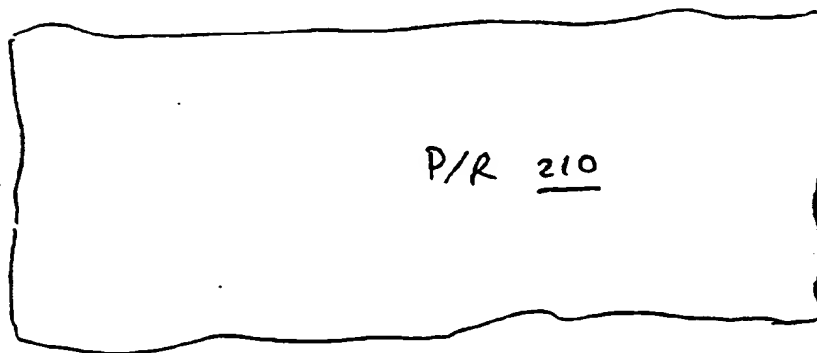


Fig. 2b

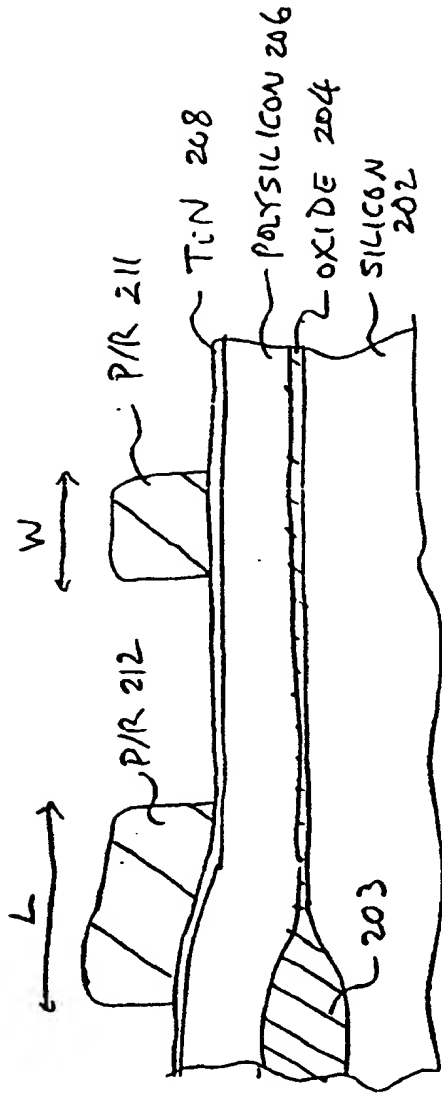


Fig. 2c

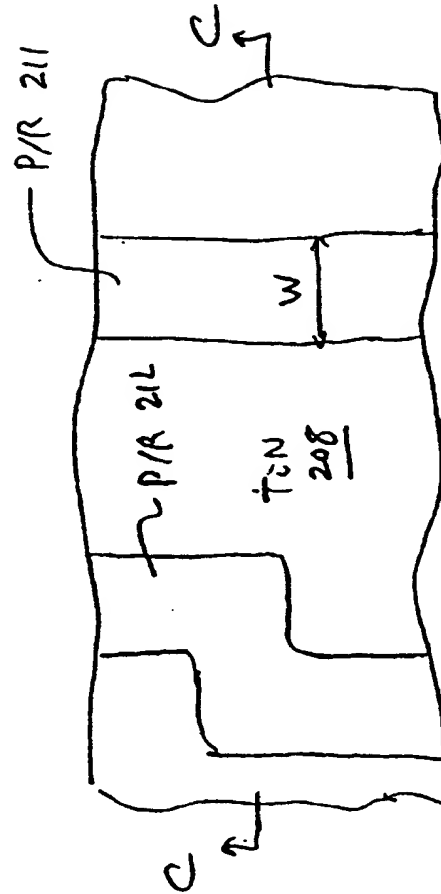


Fig. 2d.

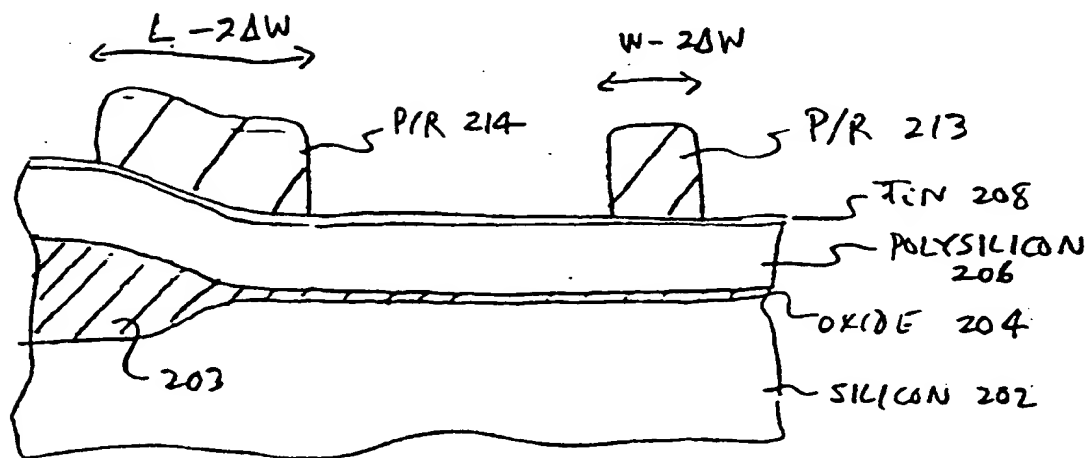


Fig. 2e

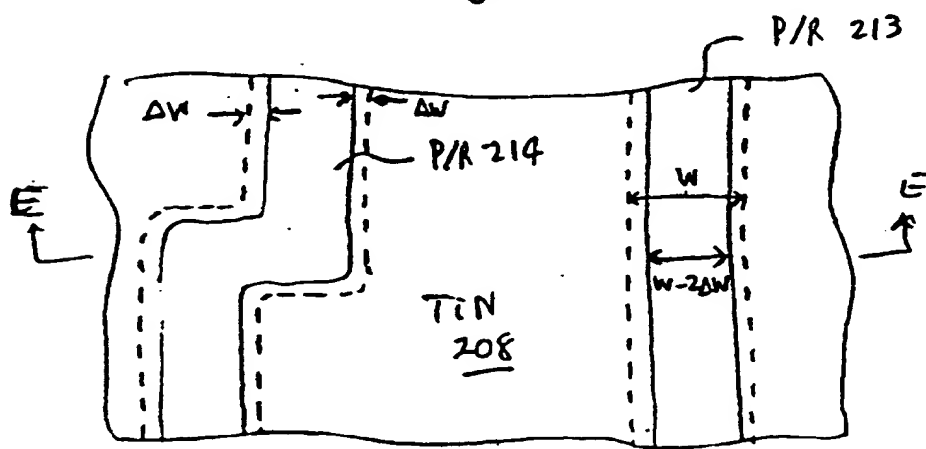


Fig. 2f

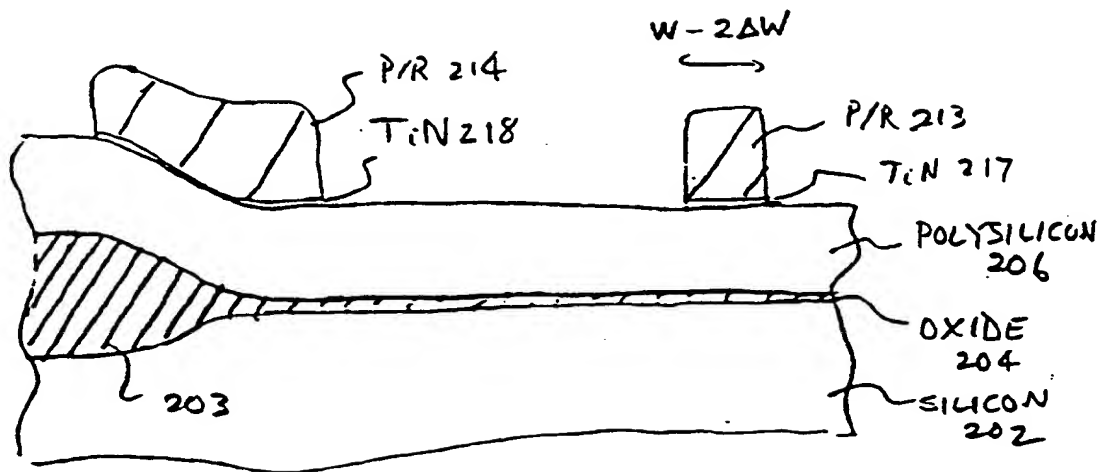


Fig. 2g

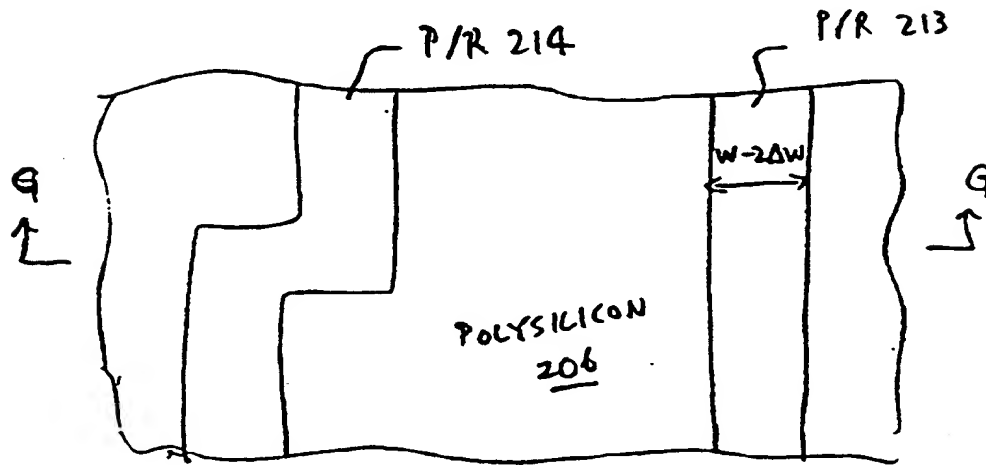


Fig. 2h.

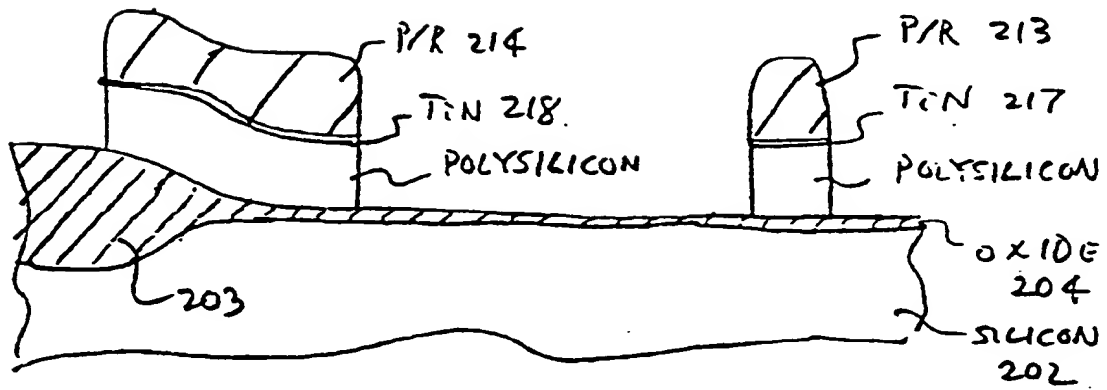


Fig. 3

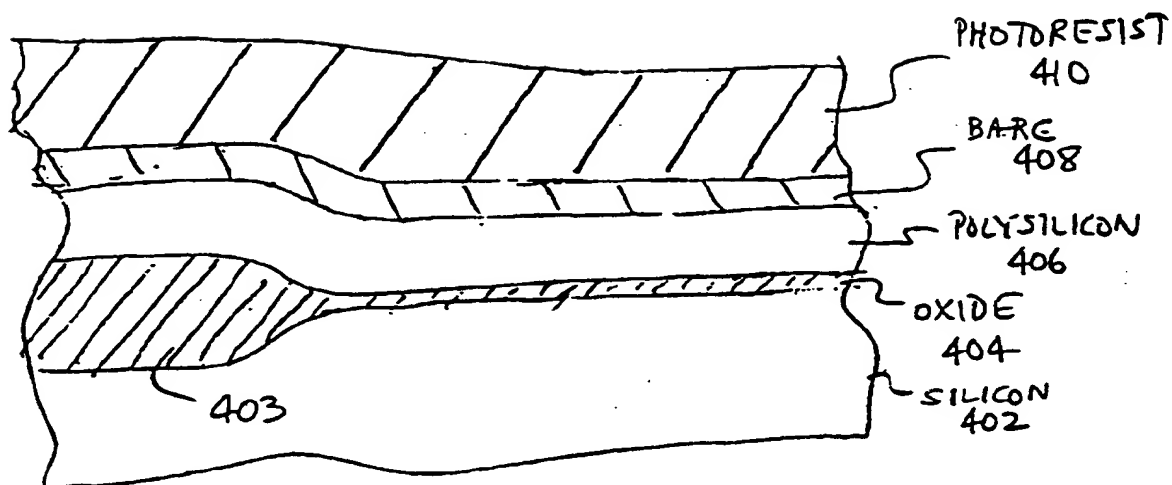


Fig. 4a

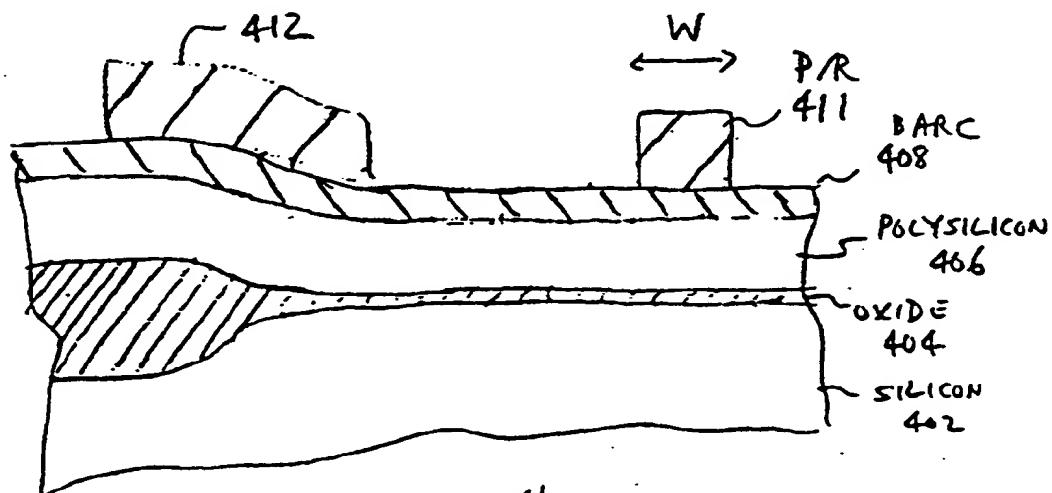


Fig. 4b

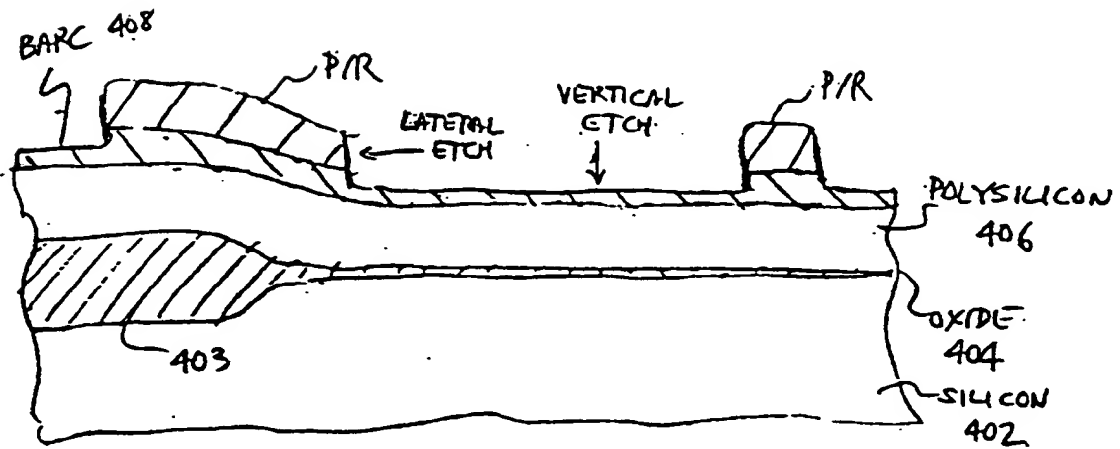


Fig. 4c

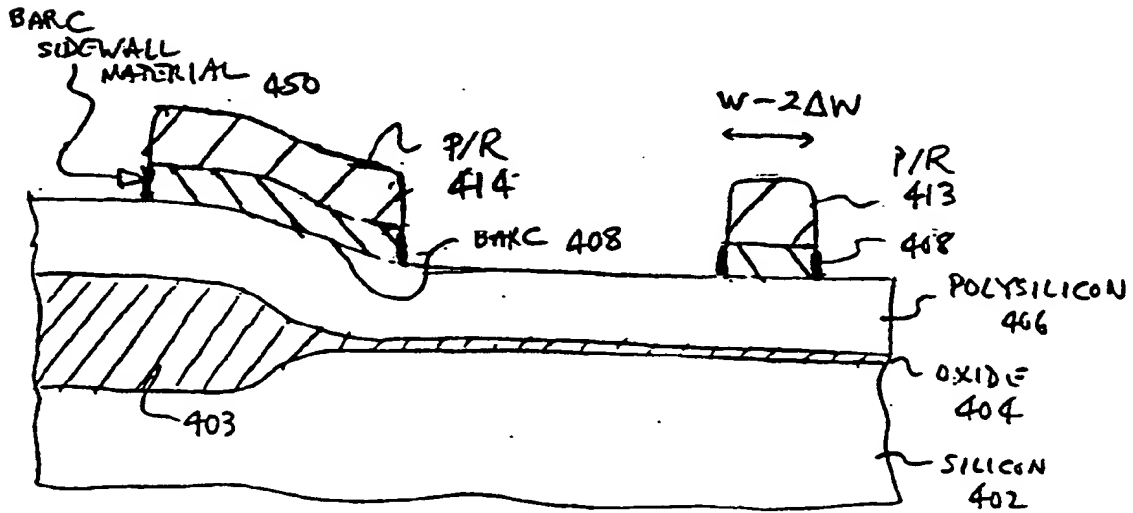


Fig. 4d

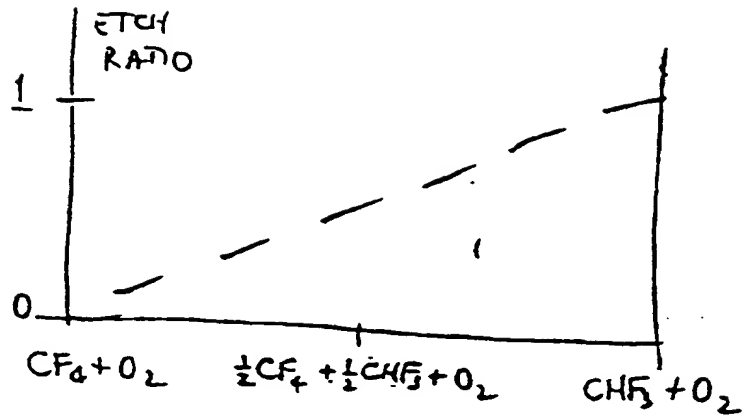


Fig. 5

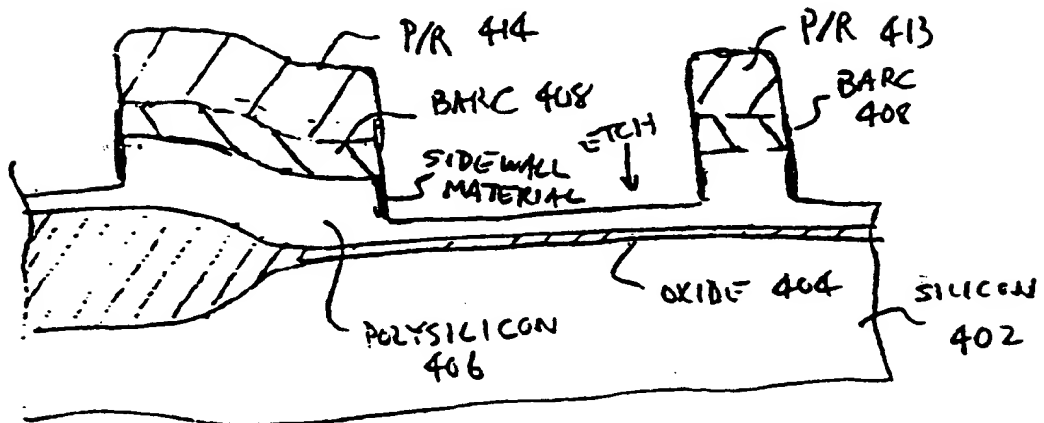


Fig. 6

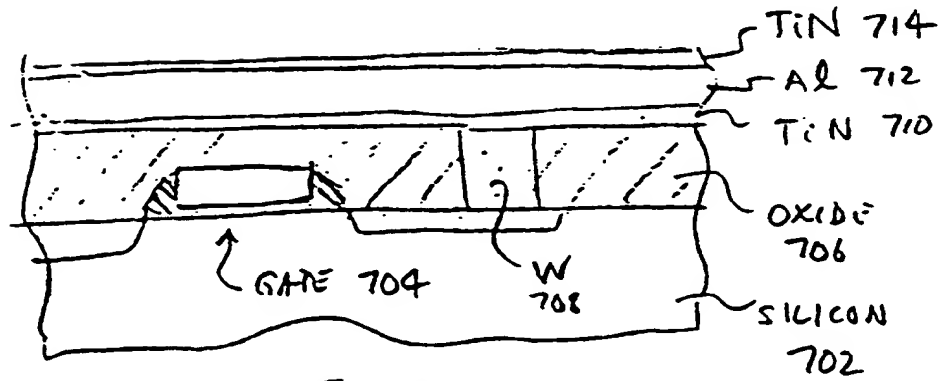


Fig. 7a

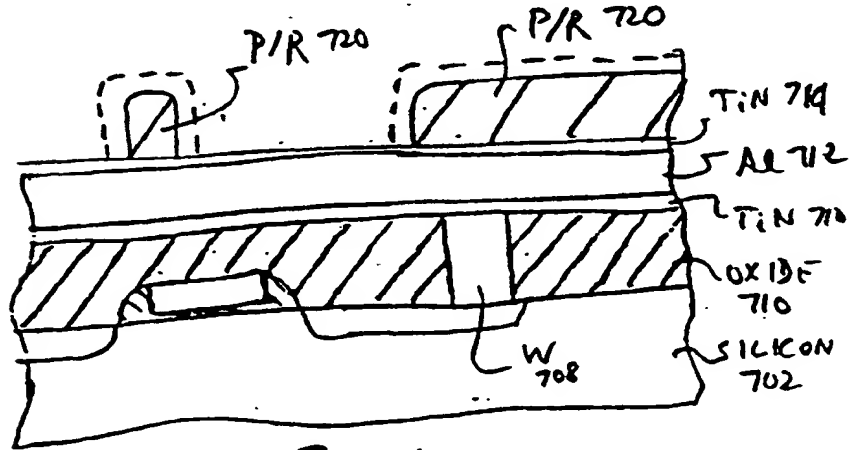


Fig. 7b

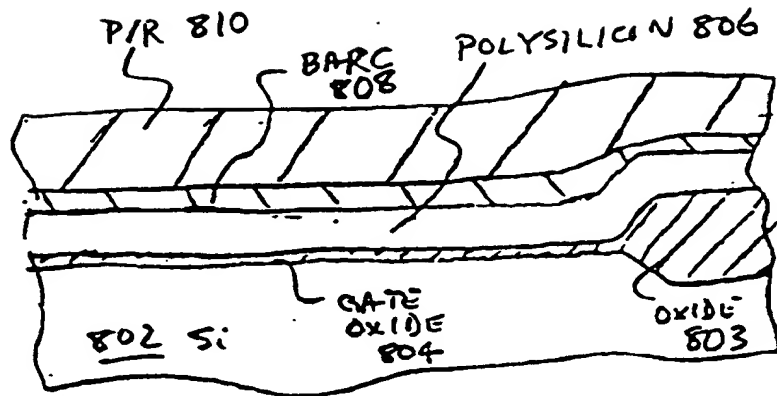


Fig. 8a

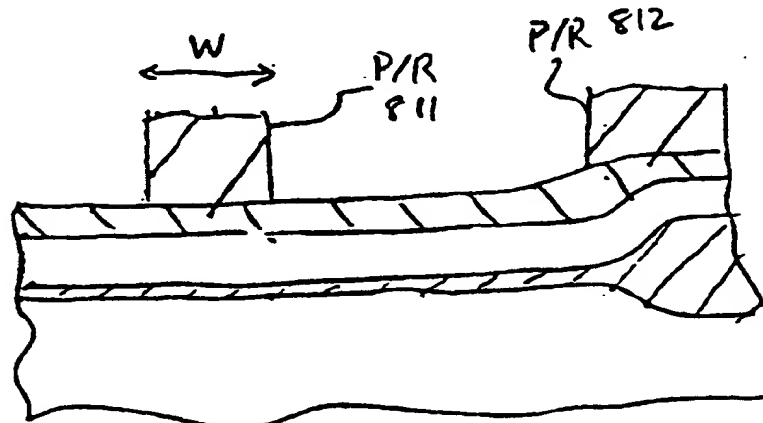


Fig. 8b

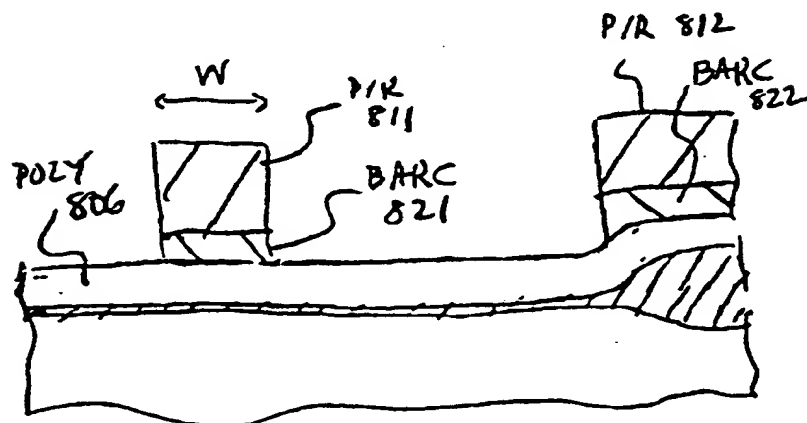


Fig. 8c

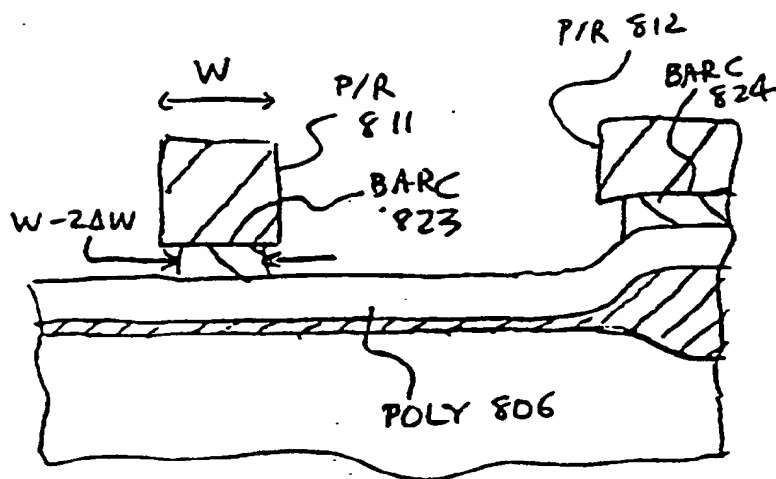


Fig. 8d

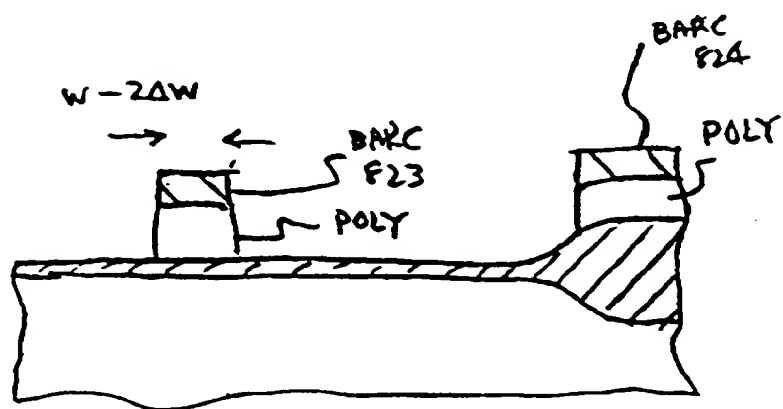


Fig. 8e

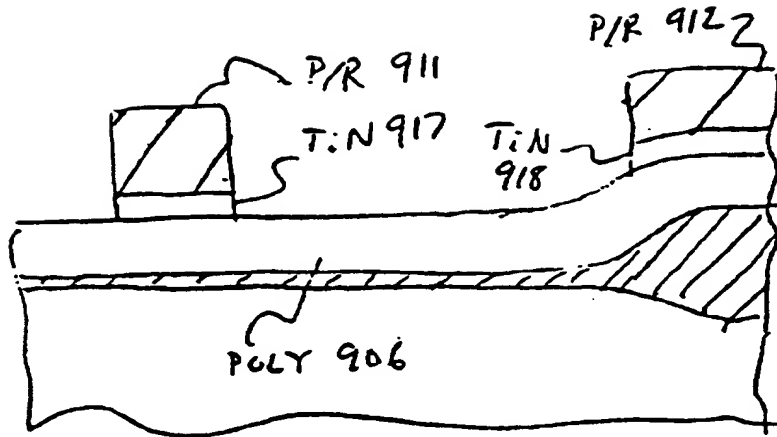


Fig. 9a

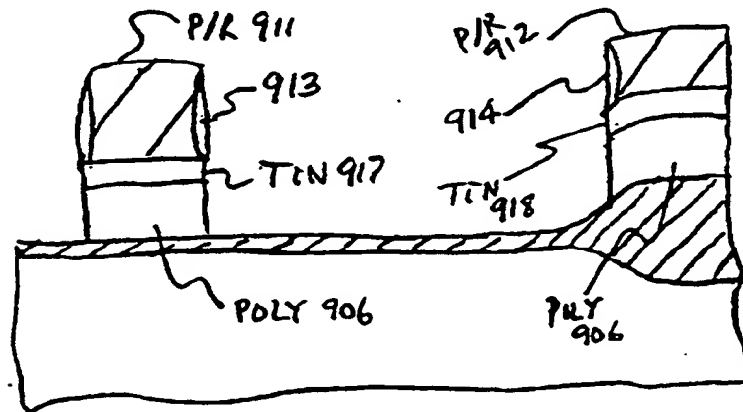


Fig. 9b

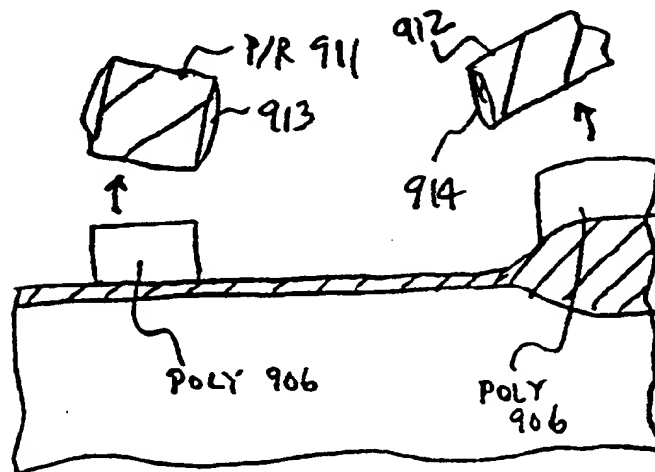


Fig. 9c

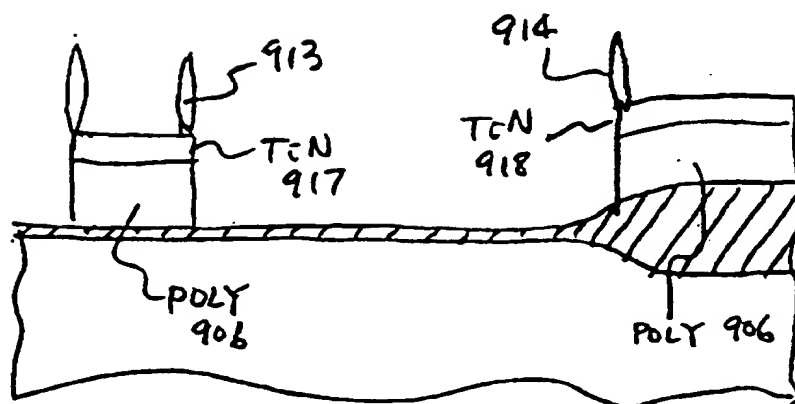


Fig. 9d



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EUROPEAN SEARCH REPORT

Application Number
EP 96 11 1356

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 471 185 (IBM) 19 February 1992 * column 4 - column 5; claims 1,5; figures 1-4 *	1-12, 17-20	H01L21/027 H01L21/268
X	US-A-5 106 786 (BRADY MICHAEL F ET AL) 21 April 1992 * claims 1,2; figures 1-4 *	1,2	
X	EP-A-0 470 707 (AMERICAN TELEPHONE & TELEGRAPH) 12 February 1992 * column 2, line 39 - column 3, line 55; figures 1-5 *	1,2, 6-14, 17-21	
X	US-A-4 820 611 (ARNOLD III WILLIAM H ET AL) 11 April 1989 * column 3 - column 4 *	1-4, 6-14, 17-21	
P,X	US-A-5 525 542 (MANIAR PAPU D ET AL) 11 June 1996 * claims 1-8; figures 1-5 *	1-4, 6-14, 17-21	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	SZE S.M. : "VLSI TECHNOLOGY. " 1985, MCGRAW-HILL, SINGAPORE XP002013182 * page 305 - page 310 *	1,2,4,5, 8,9,13, 15-18	
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The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 12 September 1996	Examiner Harmel, E
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

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